TITLE OF THE INVENTION

IMAGING DEVICE THAT PREVENTS LOSS OF SHADOW DETAIL

BACKGROUND OF THE INVENTION

5 (1) Field of the Invention

The present invention relates to an imaging device formed by one-dimensionally or two-dimensionally arranging on a semiconductor substrate a plurality of unit cells that subject incident light to photoelectric conversion. In particular,

10 the present invention relates to a technique for preventing loss of shadow detail in an image underexposed due to strong incident light.

(2) Related Art

15 In recent years, such imaging devices as home video cameras and digital still cameras have been popularly widespread.

Theses imaging devices may include an image sensor featuring an amplifier.

20 Although having advantageous characteristics such as low noise, an image sensor featuring an amplifier suffers from the problem that underexposure occurs due to strong incident light, resulting in loss of shadow detail of an image.

Japanese Laid-Open Patent Application No. 2000-287131

25 describes an overview of a CMOS image sensor that is an image

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sensor featuring an amplifier, discusses the problem mentioned above, and discloses a CMOS image sensor that can solve the above problem by detecting, for each pixel sensor, strong incident light based on an output voltage at reset, and replacing the output voltage at reset with another voltage.

According to Japanese Laid-Open Patent Application No. 2000-287131, an output voltage at reset is used to detect a pixel sensor for which shadow detail loss of an image may occur. A change in the output voltage at reset however is a direct cause for shadow detail loss of an image. Even a subtle change in the output voltage at reset directly affects brightness information.

Such a change in an output voltage at reset can be detected only when the change is large enough to be detected. It is therefore impossible to completely eliminate an adverse effect by such a change in an output voltage at reset.

Further, an output voltage at reset changes acutely when strong light is incident. Therefore, accurate detection of such a change is not easy, and thus effectively preventing shadow detail loss of an image is not an easy task.

Assume for example that a photograph of a subject composed of a sufficiently bright middle portion and surrounding peripheral portions that get gradually darker as closer to the edge of the subject is taken by the CMOS image sensor disclosed in Japanese Laid-Open Patent Application No.

2000-287131.   In this case, the image sensor can prevent underexposure in the sufficiently bright middle portion, but fails to prevent underexposure in a peripheral portion surrounding the middle portion, so that the peripheral portion surrounding the middle portion appears to be darker than a further peripheral portion closer to the edge. Depending on the degree of underexposure occurring in the peripheral portion appearing darker, this portion may be viewed as a ring-shaped black area in which shadow detail is lost.

SUMMARY OF THE INVENTION

In view of the above problem, the object of the present invention is to provide an imaging device and an imaging method that can effectively prevent loss of shadow detail in an image underexposed due to strong incident light compared with conventional imaging devices, and can ensure elimination of an adverse effect by a change in a voltage at reset.

The object of the present invention can be achieved by an imaging device that outputs brightness information according to an amount of incident light, including: an imaging unit that includes a plurality of unit cells arranged one dimensionally or two-dimensionally, each unit cell including a photoelectric conversion part that generates a first output voltage in a reset state and a second output voltage according to an amount of incident light, and each unit cell generating

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a reset voltage that corresponds to the first output voltage and a read voltage that corresponds to the second output voltage; and an output unit operable to output, in relation to each unit cell, brightness information indicating a difference between the reset voltage and the read voltage when the read voltage is in a predetermined range, and brightness information indicating high brightness when the read voltage is not in the predetermined range.

The object of the present invention can also be achieved by an imaging method for use in an imaging device that includes an imaging area formed by a plurality of unit cells arranged one dimensionally or two-dimensionally, and outputs brightness information according to an amount of incident light, each unit cell including a photoelectric conversion part that generates a first output voltage in a reset state and a second output voltage according to an amount of incident light, and each unit cell generating a reset voltage corresponding to the first output voltage and a read voltage corresponding to the second output voltage, the method including: a judgment step of judging, in relation to each unit cell, whether the read voltage is in a predetermined range; a first output step of outputting brightness information indicating a difference between the reset voltage and the read voltage when the read voltage is judged to be in the predetermined range; and a second output step of

outputting brightness information indicating high brightness when the read voltage is judged not to be in the predetermined range.

According to these, the voltage at reading is used to detect a pixel sensor for which shadow detail loss of an image may occur. This means that a preventive measure against shadow detail loss is taken even for incident light much weaker than such strong light that causes a change in a voltage at reset, which is a direct cause of shadow detail loss, etc.

Accordingly, the imaging device can effectively solve the problem of shadow detail loss in an image underexposed due to strong incident light compared with conventional cases, and can ensure elimination of an adverse effect by a change in a voltage at reset.

In the imaging device, the output unit may include: a first output line that is connected to the imaging unit and receives the reset voltage and the read voltage output from each unit cell; a second output line that is connected to a circuit of a subsequent stage and outputs brightness information to the circuit of the subsequent stage; a clamp capacitance that is connected in series between the first output line and the second output line; and a bypass transistor that is connected in parallel with the clamp capacitance, and brings the first output line and the second output line out of conduction not to bypass the clamp capacitance in a

first case where a voltage applied between terminals of the clamp capacitance is in the predetermined range, and brings the first output line and the second output line into conduction to bypass the clamp capacitance in a second case where the voltage applied between the terminals is not in the predetermined range.

According to this construction, when a voltage applied between the terminals of the clamp capacitance is not in the predetermined range, the voltage of the second output line is replaced by the voltage of the first output line without requiring any special operation. The resulting voltage is then output as brightness information. Therefore, the object can be achieved simply by providing one bypass transistor for each output unit.

In the imaging device, the first case may be where an electric potential of the first output line is higher than a barrier potential of the bypass transistor, and the second case may be where the electric potential of the first output line is equal to or smaller than the barrier potential of the bypass transistor.

According to this construction, when the electric potential of the first output line is higher than the barrier potential of the bypass transistor, the voltage of the second output line is replaced by the voltage of the first output line without requiring any special operation. The resulting

voltage is then output as brightness information. Therefore, the object can be achieved simply by providing one bypass transistor for each output unit.

In the imaging device, the output unit further may include: a sampling capacitance that is connected in series between the second output line and a terminal for supplying a predetermined voltage; a clamp transistor that is connected in series between the second output line and a terminal for supplying a reference voltage; and a control unit operable to control a reset voltage to be output to the first output line in a state where the clamp transistor is ON and the second output line is set at the reference voltage, and then control a read voltage to be output to the first output line in a state where the clamp transistor is OFF, and wherein when a reset voltage that is in the predetermined range is output to the first output line in a state where the clamp transistor is ON and the second output line is set at the reference voltage, an equivalent to a difference between the reference voltage and the reset voltage may be held by the clamp capacitance, and then when a read voltage that is in the predetermined range is output to the first output line in a state where the clamp transistor is OFF, a voltage of the second output line may change from the reference voltage by an amount corresponding to the equivalent held by the clamp capacitance, so that brightness information indicating a difference

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between the reset voltage and the read voltage is output, and when a read voltage that is not in the predetermined range is output to the first output line in a state where the clamp transistor is OFF, the bypass transistor may bring the first output line and the second output line into conduction to bypass the clamp capacitance and so the voltage of the second output line is replaced by the read voltage, so that brightness information indicating high brightness is output regardless of whether the reset voltage is in the predetermined range.

In the imaging device, the output unit may further include: a sampling capacitance that is connected in series between the second output line and a terminal for supplying a predetermined voltage; a clamp transistor that is connected in series between the second output line and a terminal for supplying a reference voltage; and a control unit operable to switch the clamp transistor ON in a state where a read voltage is output to the first output line, and then switch the clamp transistor OFF and controls a reset voltage to be output to the first output line, and wherein when the clamp transistor is switched ON in a state where a read voltage that is in the predetermined range is output to the first output line, an equivalent to a difference between the reference voltage and the read voltage may be held by the clamp capacitance, and then the clamp transistor may be switched OFF and a reset voltage that is in the predetermined

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range is output to the first output line, and a voltage of the second output line may change from the reset voltage by an amount corresponding to the equivalent held by the clamp capacitance, so that brightness information indicating a

5   difference between the reset voltage and the read voltage is output, and the bypass transistor may bring the first output line and the second output line into conduction to bypass the clamp capacitance in a state where a read voltage that is not in the predetermined range is output to the first output

10   line and so no voltage is held by the clamp capacitance, so that brightness information indicating high brightness is output.

According to these, when the read voltage is not in the predetermined range, the voltage of the second output line

15   is replaced by the read voltage. The resulting voltage is then output as brightness information. Therefore, the object can be achieved simply by providing one bypass transistor for each output unit.

In the imaging device, the output unit may further include

20   a voltage supplying unit operable to supply a bias voltage to a gate of the bypass transistor.

According to this construction, dynamic characteristics of the bypass transistor can be adjusted by the bias voltage supplied, depending on individual cases or even after its

25   manufacture. Due to this, high versatility can be realized.

In the imaging device, the bypass transistor may be a depletion-mode transistor.

According to this construction, a bias voltage does not need to be supplied to the bypass transistor. Therefore, the circuit configuration can be simplified.

In the imaging device, each unit cell may include: a light-receiving element operable to generate charge according to an amount of incident light; a charge detecting unit operable to hold the charge generated by the light-receiving element and output the charge as a voltage signal; a reset transistor that is connected in series between a reset terminal for supplying a reference voltage and the charge detecting unit, and when a gate voltage is applied thereto, the reset transistor is brought into conduction, so that the charge detecting unit is reset to the reference voltage; and an amplifier transistor that is connected between an amplifier terminal for supplying a reference voltage and the first output line, and when a voltage signal converted by the charge detecting unit is applied to a gate thereof, the voltage signal is amplified and the amplified voltage signal is output to the first output line, and wherein a barrier potential of the bypass transistor may be higher by a predetermined amount than an electric potential of a saturation signal that is an output of the amplifier transistor and that depends on an electric potential of the reset transistor being out of conduction.

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According to this construction, when a difference between the barrier potential of the bypass transistor and the electric potential of the saturation signal is larger than a predetermined value, the bypass transistor works, thereby producing an expected effect.

In the imaging device, a difference between the barrier potential of the bypass transistor and the electric potential of the saturation signal may be substantially 0.1V.

According to this construction, a difference between the barrier potential of the bypass transistor and the electric potential of the saturation signal is set at substantially 0.1V.

In the imaging device, the output unit may further include a voltage supplying unit operable to supply a bias voltage to a gate of the bypass transistor, and wherein a difference between the barrier potential of the bypass transistor and the electric potential of the saturation signal may be set by the bias voltage.

According to this construction, a difference between the barrier potential of the bypass transistor and the electric potential of the saturation signal can be set by the bias voltage supplied.

In the imaging device, the bypass transistor and the reset transistor may be manufactured in one process.

According to this construction, the bypass transistor

and the reset transistor are manufactured in one process, and accordingly can have similar electric characteristics. The bias voltage to be supplied to each pair of a bypass transistor and a reset transistor manufactured in one process

5   can be made substantially uniform with reduced variations, and therefore, the setting of the bias voltage to be supplied can be made easy.

In the imaging device, the voltage supplying unit may include a bias setting circuit that enables an appropriate

10   bias unique to the imaging device to be set from outside.

According to this construction, the bias voltage can be set from outside. Therefore, the characteristics of imaging devices that often fail to be made uniform can be made uniform.

15   In the imaging device, the reset transistor may be manufactured by a predetermined process of burying through injection, and the bypass transistor may be manufactured by the predetermined process of burying through injection and an additional injection process, and wherein a difference

20   between the barrier potential of the bypass transistor and the electric potential of the saturation signal may be set by the additional injection process.

According to this construction, a difference between the barrier potential of the bypass transistor and the electric

25   potential of the saturation signal can be set by the additional

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injection process.

In the imaging device, a first substrate bias voltage may be applied to the bypass transistor, the first substrate bias voltage having an electric potential different from a second substrate bias voltage applied to the reset transistor, and wherein a difference between the barrier potential of the bypass transistor and the electric potential of the saturation signal may be controlled by a difference between the first substrate bias voltage and the second substrate bias voltage.

According to this construction, a difference between the barrier potential of the bypass transistor and the electric potential of the saturation signal can be set by a difference between the substrate bias voltage applied to the bypass transistor and the substrate bias voltage applied to the reset transistor.

In the imaging device, the output unit may further include a clip transistor operable to output, as brightness information indicating high brightness, a voltage matching an input dynamic range of the circuit of the subsequent stage that is an analogue circuit, when a voltage that is a difference between an electric potential of the first output line and an electric potential of the second output line is not in the predetermined range.

According to this construction, a voltage matching the

input dynamic range of the analogue circuit of the subsequent stage can be output as brightness information indicating high brightness. Therefore, performance of the analogue circuit can be efficiently utilized.

In the imaging device, the clip transistor may be connected between a terminal for supplying a voltage corresponding to a maximum voltage of the input dynamic range of the circuit of the subsequent stage and the second output line, and when a predetermined voltage is applied to a gate thereof, the clip transistor may be temporarily brought into conduction, so that a voltage matching the input dynamic range is output from the second output line to the circuit of the subsequent stage, and the output unit may further include a clip transistor control unit operable to pulse drive the clip transistor by temporarily bringing the clip transistor into conduction, where a pulse voltage is applied to a gate of the clip transistor when the circuit of the subsequent stage inputs the brightness information.

According to this construction, the clip transistor can be pulse driven, and therefore, power consumption can be made low.

In the imaging device, the output unit may further include; a sampling transistor that is connected in series between the first output line and the clamp capacitance; and a sampling transistor control unit operable to bring the

sampling transistor out of conduction in a vertical blanking period during which brightness information is not output from the imaging unit.

According to this construction, the sampling transistor can be brought out of conduction during the vertical blanking period, and so the first output line and the clamp capacitance can be brought out of conduction. Therefore, no charge is held by the clamp capacitance. As a result, brightness information indicating low brightness can be output.

Accordingly, a saturation signal is not output during the vertical blanking period. Therefore, an input dynamic range of an output amplifier of the subsequent stage is not restricted.

In the imaging device, each unit cell may include: an amplifier transistor that is connected in series between an amplifier terminal for supplying a reference voltage and the first output line, and when a voltage signal converted by a charge detecting unit is applied to a gate thereof, the voltage signal is amplified and the amplified voltage signal is output to the first output line; and a select transistor that is connected in series between the amplifier terminal and the amplifier transistor or between the amplifier transistor and the first output line, and the output unit may further include: a load transistor operable to read the output voltage via the amplifier transistor and the select

transistor by loading the first output line when the load transistor is in conduction; and a control unit operable to (a) bring a select transistor included in one or more of the unit cells into conduction before bringing the load transistor

5   into conduction, (b) bring the load transistor out of conduction before bringing select transistors included in all the unit cells out of conduction, and (c) bring the load transistor out of conduction during a vertical blanking period during which brightness information is not output from any

10   of the unit cells.

　　　　According to this construction, the load transistor can be brought out of conduction during the vertical blanking period. Therefore, no charge is held by the clamp capacitance. As a result, brightness information indicating low brightness

15   can be output.

　　　　Accordingly, a saturation signal is not output during the vertical blanking period. Therefore, an input dynamic range of an output amplifier of the subsequent stage is not restricted.

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BRIEF DESCRIPTION OF THE DRAWINGS

　　　　These and other objects, advantages and features of the invention will become apparent from the following description thereof taken in conjunction with the accompanying drawings

25   that illustrate a specific embodiment of the invention.

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In the drawings:

FIG. 1 shows a schematic construction of an imaging device relating to a first embodiment of the present invention;

FIG. 2 shows a schematic circuit configuration of the imaging device relating to the first embodiment;

FIG. 3 shows the timings of various control pulses supplied in the imaging device relating to the first embodiment;

FIGS. 4A to 4D each show the state of electric potential in each area of a pixel circuit 110 at each timing in the normal case;

FIG. 5A shows the state of electric potential in each area of a signal processing circuit 120 at the timing "b" in FIG. 3 in the normal case;

FIG. 5B shows the state of electric potential in each area of the signal processing circuit 120 at the timing "b'" in FIG. 3 in the normal case;

FIG. 5C shows the state of electric potential in each area of the signal processing circuit 120 at the timing "d" in FIG. 3 in the normal case;

FIGS. 6A to 6D, and FIG. 7 each show the state of electric potential in each area of the pixel circuit 110 at each timing in the high brightness case;

FIG. 8A shows the state of electric potential in each area of the signal processing circuit 120 at the timing "b"

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in FIG. 3 in the first high-brightness case;

FIG. 8B shows the state of electric potential in each area of the signal processing circuit 120 at the timing "b'" in FIG. 3 in the first high-brightness case;

FIG. 8C shows the state of electric potential in each area of the signal processing circuit 120 at the timing "d" in FIG. 3 in the first high-brightness case;

FIG. 9A shows the state of electric potential in each area of the signal processing circuit 120 at the timing "b" in FIG. 3 in the second high-brightness case;

FIG. 9B shows the state of electric potential in each area of the signal processing circuit 120 at the timing "b'" in FIG. 3 in the second high-brightness case;

FIG. 9C shows the state of electric potential in each area of the signal processing circuit 120 at the timing "d" in FIG. 3 in the second high-brightness case;

FIG. 10A shows characteristics of a voltage of a first signal output line at reset;

FIG. 10B shows characteristics of a voltage of the first signal output line at reading;

FIG. 10C shows characteristics of an output voltage of a conventional imaging device without any measures taken to prevent underexposure or shadow detail loss of an image, corresponding to FIGS 10A and 10B;

FIG. 10D shows characteristics of an output voltage of

the imaging device relating to the first embodiment;

FIG. 11 shows a schematic circuit configuration of an imaging device relating to a second embodiment of the present invention;

FIG. 12 shows the timings of various control pulses including a clip pulse when a clip transistor 131 included in the imaging device relating to the second embodiment is pulse driven;

FIG. 13 shows the state of electric potential in each area of a signal processing circuit 130 at the timing "d" in FIG. 3 in the high brightness case;

FIG. 14A shows the state of electric potential in each area of the signal processing circuit 130 at the timing "d" in FIG. 12 in the high brightness case;

FIG. 14B shows the state of electric potential in each area of the signal processing circuit 130 at the timing "e" in FIG. 12 in the high brightness case;

FIG. 15 shows a circuit configuration of an imaging device relating to a third embodiment of the present invention;

FIG. 16 shows the timings of various control pulses supplied in the imaging device relating to the third embodiment;

FIGS. 17A to 17D each show the state of electric potential in each area of a pixel circuit 140 at each timing in the normal case;

FIG. 18A shows the state of electric potential in each area of a signal processing circuit 150 at the timing "a" in FIG. 16 in the normal case;

FIG. 18B shows the state of electric potential in each area of the signal processing circuit 150 at the timing "b" in FIG. 16 in the normal case;

FIG. 18C shows the state of electric potential in each area of the signal processing circuit 150 at the timing "d" in FIG. 16 in the normal case;

FIGS. 19A to 19D each show the state of electric potential in each area of the pixel circuit 140 at each timing in the high brightness case;

FIG. 20A shows the state of electric potential in each area of the signal processing circuit 150 at the timing "a" in FIG. 16 in the high brightness case;

FIG. 20B shows the state of electric potential in each area of the signal processing circuit 150 at the timing "b" in FIG. 16 in the normal case;

FIG. 20C shows the state of electric potential in each area of the signal processing circuit 150 at the timing "d" in FIG. 16 in the normal case;

FIGS. 21A and 21B each show the relationship between a barrier potential of a reset transistor and a barrier potential of a bypass transistor;

FIG. 22 shows the timings of a sampling pulse relating

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to modification 2; and

FIG. 23 shows the timings of control over a load transistor relating to modification 3.

5   DESCRIPTION OF THE PREFERRED EMBODIMENTS

[First Embodiment]

FIG. 1 shows a schematic construction of an imaging device relating to a first embodiment of the present invention.

As shown in FIG. 1, the imaging device relating to the

10   first embodiment includes an imaging unit 1, a load circuit unit 2, a line select encoder 3, a column select encoder 4, a signal processing unit 5, and an output circuit 6.

The imaging unit 1 is an imaging area formed by one-dimensionally or two-dimensionally arranging a plurality

15   of unit cells. Here, the imaging unit 1 is described as being composed of nine pixels arranged two-dimensionally in a 3 x 3 matrix for convenience, but is actually composed of about several thousands pixels in the case of one-dimensional arrangement, and about several hundreds of thousands to

20   several millions pixels in the case of two-dimensional arrangement.

The load circuit unit 2 is formed by connecting the same circuits corresponding in one-to-one to columns. The load circuit 2 loads, in units of columns, the pixels of the imaging

25   unit 1 on every reading of an output voltage.

The line select encoder 3 includes three control lines "RESET", "READ", and "LSEL" corresponding in one-to-one to lines. The line select encoder 3 controls, in units of lines, the pixels of the imaging unit 1 to be reset, read, or selected.

5   The column select encoder 4 includes control lines, and sequentially selects columns.

The signal processing unit 5 is formed by connecting the same circuits corresponding in one-to-one to columns. The signal processing unit 5 processes outputs made in units

10   of columns from the imaging unit 1, and sequentially outputs the resulting data.

The output circuit 6 subjects outputs of the signal processing unit 5 to necessary conversion, and outputs the resulting data to outside.

15   FIG. 2 shows a schematic circuit configuration of the imaging device relating to the first embodiment.

As shown in FIG. 2, the imaging device relating to the first embodiment includes a load circuit 100, a pixel circuit 110, and a signal processing circuit 120.

20   The load circuit 100 is one of the circuits constituting the load circuit unit 2 shown in FIG. 1. The load circuit 100 includes a load transistor 101 connected between a first signal output line and a GND, and supplies a load voltage (LG).

25   The pixel circuit 110 is one of the unit cells

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constituting the imaging unit 1 shown in FIG. 1. The pixel circuit 110 is characterized by outputting a reset voltage obtained by amplifying a voltage at reset and a read voltage obtained by amplifying a voltage at reading, to the first

5   signal output line. The pixel circuit 110 includes a light-receiving element 111 such as a photodiode that subjects incident light to photoelectric conversion and outputs charge, a capacitor 112 that accumulates the charge generated by the light-receiving element 111 and outputs the accumulated charge

10   as a voltage signal, a reset transistor 113 that resets a voltage indicated by the capacitor 112 to an initialization voltage (*VDD* here), a read transistor 114 that supplies the charge output by the light-receiving element 111 to the capacitor 112, an amplifier transistor 115 that outputs a

15   voltage that follows the voltage indicated by the capacitor 112, and a line select transistor 116 that outputs an output of the amplifier transistor 115 to the first signal output line upon receipt of a line select signal from the line select encoder 3. In this specification, for ease of explanation,

20   a point in the capacitor 112 indicating a voltage determined according to the accumulated charge of the capacitor 112, and where the reset transistor 113, the read transistor 114, and the amplifier transistor 115 are connected is hereafter referred to as a charge detecting unit 117.

25   The signal processing circuit 120 is one of the circuits

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constituting the signal processing unit 5 shown in FIG. 1. The signal processing circuit 120 is characterized by outputting brightness information indicating a difference between a reset voltage output from the unit cell and a read

5 voltage when the read voltage is in a predetermined range, and outputting brightness information indicating high brightness when the read voltage is not in the predetermined range. The signal processing circuit 120 includes a sampling transistor 121 and a clamp capacitance 122 connected in series

10 between the first signal output line and the second signal output line, a sampling capacitance 123 connected in series between the second signal output line and the GND, a clamp transistor 124 connected in series between the second signal output line and a reference voltage terminal *VDD*, and a bypass

15 transistor 125 that is connected in parallel with the clamp capacitance 122 and that brings the first signal output line and the second signal output line out of conduction not to bypass the clamp capacitance 122 when a voltage applied between the terminals of the clamp capacitance 122 does not exceed

20 the predetermined voltage, and brings the first signal output line and the second signal output line into conduction to bypass the clamp capacitance 122 when the voltage exceeds the predetermined voltage.

Here, to the pixel circuit 110, a reset pulse

25 (initialization signal: RESET), a read pulse (READ), a line

select signal (LSEL) are supplied at predetermined timings, and to the signal processing circuit 120, a sampling pulse (SP) and a clamp pulse (CP) are supplied at predetermined timings. Transistors corresponding to these control pulses are switched ON and OFF.

FIG. 3 shows the timings of various control pulses supplied in the imaging device relating to the first embodiment.

By supplying the control pulses at the timings shown in FIG. 3, the clamp transistor 124 can be switched ON with the line select transistor 116 being ON, and the reset voltage can be output to the first signal output line with the second signal output line being set at a reference voltage ("a" in FIG. 3). Here, when the reset voltage is in a predetermined range, an equivalent to a difference between the reference voltage and the reset voltage is held by the clamp capacitance 122 ("b" in FIG. 3). After this, the read voltage is output to the first signal output line with the clamp transistor 124 being OFF ("c" in FIG. 3). Here, when the read voltage is in a predetermined range, the voltage of the second signal output line changes from the reference voltage by an amount equivalent to a difference between the reset voltage and the read voltage ("d" in FIG. 3). The resulting voltage can then be output as brightness information. When the read voltage is not in a predetermined range, the bypass transistor 125

brings the first signal output line and the second signal output line into conduction to bypass the clamp capacitance 122, so that the voltage of the second signal output line is replaced by the read voltage. The resulting voltage can

5 then be output as brightness information.

Here, the predetermined voltage range may be set by incorporating a depletion-mode transistor as the bypass transistor 125 during the manufacture, or by supplying, with the use of voltage supplying means, a bias voltage constantly

10 or at necessary timings ("c" to "d" in FIG. 3 etc.) to the gate of the bypass transistor 125.

As one example, the bias voltage may be output, in the form of pulses, to the gate of the bypass transistor 125 during when the read voltage is being read from the pixel circuit

15 110.

<Operations>

FIGS. 4A to 4D each show the state of electric potential in each area of the pixel circuit 110 at each timing in the

20 case where such strong light that causes underexposure or loss of shadow detail of an image is not incident (hereafter referred to as the "normal case").

FIGS. 4A to 4D respectively correspond to the timings "a" to "d" in FIG. 3.

25 FIG. 5A shows the state of electric potential in each

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area of the signal processing circuit 120 at the timing "b"
in FIG. 3.

FIG. 5B shows the state of electric potential in each
area of the signal processing circuit 120 at the timing "b'"
in FIG. 3.

FIG. 5C shows the state of electric potential in each
area of the signal processing circuit 120 at the timing "d"
in FIG. 3.

Here, FIGS. 4A to 4D and FIGS. 5A to 5C each show in
its upper half a schematic circuit construction and in its
lower half the state of electric potential in the areas
corresponding to the positions in the circuit shown in the
upper half.

The following describes the change of electric potential
in each area of the pixel circuit 110 and the change of electric
potential in each area of the signal processing circuit 120,
with reference to FIGS. 4A to 4D and FIGS. 5A to 5C.

(1) At the timing "a" in FIG. 3, the read transistor
114 is OFF and the reset transistor 113 is ON. Therefore,
as shown in FIG. 4A, the charge generated in the light-receiving
element 111 is not transferred to the charge detecting unit
117, and the charge of the charge detecting unit 117 is
transferred to the VDD terminal.

(2) At the timing "b" in FIG. 3, the reset transistor
113 is switched from ON to OFF. As shown in FIG. 4B, the voltage

of the charge detecting unit 117 is reset to the *VDD*. Also, as shown in FIG. 5A, because the clamp transistor 124 is ON, the voltage of the second signal output line is reset to the *VDD*.

5   (3) At the timing "b'" in FIG. 3, the clamp transistor 124 is switched from ON to OFF. As shown in FIG. 5B, an equivalent to a difference between the reset voltage and the *VDD* is held by the clamp capacitance 122.

        (4) At the timing "c" in FIG. 3, the read transistor
10   114 is switched ON, with the reset transistor 113 being OFF. Therefore, as shown in FIG. 4C, the charge generated in the light-receiving element 111 is transferred to the charge detecting unit 117.

        (5) At the timing "d" in FIG. 3, as shown in FIG. 4D,
15   the read transistor 114 is switched OFF, with the reset transistor 113 being OFF. Therefore, the charge generated in the light-receiving element 111 is read to the charge detecting unit 117.

        Here, the voltage of the charge detecting unit 117 changes,
20   and the resulting voltage is amplified by the amplifier transistor 115. Therefore, the voltage of the first signal output line changes to the read voltage. Also, because the equivalent to the difference between the reset voltage and the *VDD* is held by the clamp capacitance 122, the voltage
25   of the second signal output line becomes a voltage obtained

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by subtracting the voltage change of the first signal output line from the VDD as shown in FIG. 5C. The resulting voltage is then output as brightness information (assuming the voltage change of the first signal output as SIG, the clamp capacitance 122 as Ccp, and the sampling capacitance 123 as Csp, the voltage of the second signal output line is $VDD-SIG \times Ccp/(Ccp+Csp)$).

FIGS. 6A to 6D and FIG. 7 each show the state of electric potential in each area of the pixel circuit 110 at each timing in the case where such strong light that causes underexposure or loss of shadow detail of an image is incident (hereafter referred to as the "high brightness case").

Here, FIGS. 6A to 6D respectively correspond to the timings shown in FIG. 3A to 3D. FIG. 7 shows the case where stronger light is incident at the timing "d" in FIG. 3 than light incident in the case of FIG. 6D, or corresponds to a timing later than the timing "d" in FIG. 3. In the state shown in FIG. 7, loss of shadow detail occurs if no preventive measures are taken.

In this specification, the case where the charge of the first signal output line is not as high as to exceed the barrier potential of the bypass transistor 125 at the timing "b" in FIG. 3 in the high brightness case is specifically referred to as the "first high-brightness case", and the case where the charge of the first signal output line is as high as to exceed the barrier potential of the bypass transistor 125

at the timing "b" in FIG. 3 in the high brightness case is specifically referred to as the "second high-brightness case".

FIG. 8A shows the state of electric potential in each area of the signal processing circuit 120 at the timing "b" in FIG. 3 in the first high-brightness case.

FIG. 8B shows the state of electric potential in each area of the signal processing circuit 120 at the timing "b'" in FIG. 3 in the first high-brightness case.

FIG. 8C shows the state of electric potential in each area of the signal processing circuit 120 at the timing "d" in FIG. 3 in the first high-brightness case.

FIG. 9A shows the state of electric potential in each area of the signal processing circuit 120 at the timing "b" in FIG. 3 in the second high-brightness case.

FIG. 9B shows the state of electric potential in each area of the signal processing circuit 120 at the timing "b'" in FIG. 3 in the second high-brightness case.

FIG. 9C shows the state of electric potential in each area of the signal processing circuit 120 at the timing "d" in FIG. 3 in the second high-brightness case.

Here, FIGS. 6A to 6D, FIG. 7, FIGS. 8A to 8C, and FIG. 9A to 9C each show in its upper half a schematic circuit construction and in its lower half the state of electric potential in the areas corresponding to the positions in the circuit shown in the upper half.

The following describes the change of electric potential in each area of the pixel circuit 110 and the change of electric potential in each area of the signal processing circuit 120, with reference to FIGS. 6A to 6D, FIG. 7, FIGS. 8A to 8C, and FIGS. 9A to 9C.

(1) At the timing "a" in FIG. 3, the read transistor 114 is OFF and the reset transistor 113 is ON. Therefore, in the normal case, the charge generated in the light-receiving element 111 is not transferred to the charge detecting unit 117. In the first and second high-brightness cases as shown in FIG. 6A, however, the charge generated in the light-receiving element 111 exceeds the barrier potential of the read transistor 114, and is transferred to the charge detecting unit 117, and at the same time, the charge of the charge detecting unit 117 is transferred to the *VDD* terminal.

(2) At the timing "b" in FIG. 3, the reset transistor 113 is switched from ON to OFF. As shown in FIG. 6B, however, the charge generated in the light-receiving element 111 then exceeds the barrier potential of the read transistor 114 and is transferred to the charge detecting unit 117. Therefore, the voltage of the charge detecting unit 117 becomes lower than the *VDD*. The clamp transistor 124 is ON at this time. Therefore, in the first high-brightness case as shown in FIG. 8A, the voltage of the second signal output line is reset to the *VDD* and the charge of the first signal output line

does not exceed the barrier potential of the bypass transistor 125, and in the second high-brightness case as shown in FIG. 9A, the voltage of the second signal output line is reset to the *VDD* but at the same time the charge of the first signal output line exceeds the barrier potential of the bypass transistor 125 and is transferred to the second signal output line.

(3) At the timing "b'" in FIG. 3, the clamp transistor 124 is switched from ON to OFF. In the normal case, an equivalent to a difference between the reset voltage and the *VDD* is held by the clamp capacitance 122 with the voltage of the second signal output line being reset to the *VDD*. In the first high-brightness case as shown in FIG. 8B, however, an equivalent to a difference between the reset voltage and the *VDD*, which is smaller than that in the normal case, is held by the clamp capacitance 122, and in the second high-brightness case as shown in FIG. 9B, the charge of the first signal output line exceeds the barrier potential of the bypass transistor 125 and is transferred to the second signal output line, and substantially zero voltage difference is held by the clamp capacitance 122.

At the timings "b" and "b'" in FIG. 3, in the second high-brightness case, the charge of the first signal output line exceeds the barrier potential of the bypass transistor 125 and is transferred to the second signal output line, and

substantially zero voltage difference is held by the clamp capacitance 122. In this case, too, the resulting output becomes the same, and therefore subsequent operations are important.

5   (4) At the timing "c" in FIG. 3, the read transistor 114 is switched ON, with the reset transistor 113 being OFF. As shown in FIG. 6C, therefore, the charge generated in the light-receiving element 111 is transferred to the charge detecting unit 117.

10   (5) At the timing "d" in FIG. 3, as shown in FIG. 6D, the read transistor 114 is switched OFF, with the reset transistor 113 being OFF. Therefore, the charge generated in the light-receiving element 111 is read to the charge detecting unit 117.

15   Here, the voltage of the charge detecting unit 117 changes and the resulting voltage is amplified by the amplifier transistor 115, and therefore the voltage of the first signal output line changes to the read voltage. In the normal case, an equivalent to a difference between the reset voltage and

20   the VDD is held by the clamp capacitance 122. Therefore, the voltage of the second signal output line becomes a voltage obtained by subtracting the voltage change of the first signal output line from the VDD. The resulting voltage is then output as brightness information. In the first and second

25   high-brightness cases, however, as shown in FIGS. 8C and 9C

respectively, the charge of the first signal output line exceeds the barrier potential of the bypass transistor 125 and is transferred to the second signal output line, and the voltage of the second signal output line becomes an equivalent

5　to the voltage of the first signal output line, indicating high brightness. The resulting voltage is then output as brightness information.

<Conclusions>

10　　　FIG. 10A shows characteristics of the voltage of the first signal output line at reset.

FIG. 10B shows characteristics of the voltage of the first signal output line at reading.

FIG. 10C shows characteristics of the output voltage

15　of a conventional imaging device without any measures taken to prevent underexposure or shadow detail loss of an image, corresponding to FIGS 10A and 10B.

FIG. 10D shows characteristics of the output voltage of the imaging device relating to the first embodiment. In

20　this imaging device relating to the first embodiment, an output voltage exceeding a predetermined voltage is replaced by a voltage indicating high brightness. Therefore, underexposure or shadow detail loss of an image can be completely prevented.

25　　　Here, in FIGS. 10A to 10D, the horizontal axis indicates

strength of incident light (being stronger toward right),
and the vertical axis indicates a voltage (being more positive
toward top in FIGS. 10A and 10B, and being more negative toward
top in FIGS. 10C and 10D).

5   As described above, the first embodiment of the present
invention focuses on the voltage at reading shown in FIG.
10B. When the voltage at reading reaches a voltage in such
a range that causes the amplifier circuit to be saturated,
the bypass transistor directly replaces its output voltage
10 by a voltage indicating high brightness. In this way, the
first embodiment can effectively solve the problem of
underexposure or shadow detail loss of an image compared with
conventional cases, by taking a preventive measure even for
incident light much weaker than such incident light that causes
15 underexposure or shadow detail loss of an image. Also, the
first embodiment can ensure elimination of an adverse effect
by a change in a voltage at reset.

[Second Embodiment]
20 <Construction>
      FIG. 11 shows a schematic circuit configuration of an
imaging device relating to a second embodiment of the present
invention.

      The imaging device relating to the second embodiment
25 includes, instead of the signal processing circuit 120 in

the first embodiment, a signal processing circuit 130 that additionally includes a clip transistor 131 connected in series between the second signal output line and a clip voltage terminal (CLIPDC), to prevent the voltage of the second signal

5   output line from increasing to such a voltage that exceeds an input dynamic range of an output amplifier of the subsequent stage.

The imaging device relating to the second embodiment can regulate, with the use of the additionally provided clip

10   transistor 131, the voltage of the second signal output line so as not to be below a predetermined voltage.

Here, as a method for driving the clip transistor 131, the DC drive of applying a fixed voltage and the pulse drive of applying a clip pulse (CLIP) at appropriate timings may

15   be used.

The timings of the control pulses of various types supplied when the clip transistor 131 is DC driven are the same as the timings shown in FIG. 3 in the first embodiment.

The following describes the timings of the control pulses

20   of various types supplied when the clip transistor 131 is pulse driven.

FIG. 12 shows the timings of various control pulses including a clip pulse when the clip transistor 131 included in the imaging device relating to the second embodiment is

25   pulse driven.

As shown in FIG. 12, when the clip transistor 131 is pulse driven, the clip pulse is switched ON after the sampling pulse is switched OFF ("e" in FIG. 12), so that the voltage of the second signal output line is regulated so as not to be below a predetermined voltage. Here, the timings "a" to "d" in FIG. 12 are the same as the timings "a" to "d" in FIG. 3.

<Operation 1>

The following describes the operation when the clip transistor 131 is DC driven.

FIG. 13 shows the state of electric potential in each area of the signal processing circuit 130 at the timing "d" in FIG. 3 in the high brightness case.

Here, FIG. 13 shows in its upper half a schematic circuit configuration and in its lower half the state of electric potential in the areas corresponding to the positions in the circuit shown in the upper half.

The following describes the state of electric potential in each area of the signal processing circuit 120 in the high brightness case, with reference to FIG. 13.

(1) At the timing "d" in FIG. 3, as shown in FIG. 13, the charge of the GND exceeds the barrier potential of the load transistor 101 and is transferred to the first signal output line. Because the sampling transistor 121 is ON, the

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charge sequentially exceeds the barrier potential of each transistor and is transferred, so that a stationary current flows from the clip voltage terminal (CLIPDC) to the GND. Here, the voltage of the second signal output line is determined by the barrier potential of the clip transistor 131. This means that the voltage of the second signal output line can be set by the gate voltage of the clip transistor 131.

It should be noted here that the barrier potential of the clip transistor 131 may be set by incorporating a depletion-mode transistor as the clip transistor 131 during the manufacture.

Here, the electric potential of the first signal output line is determined by a source follower circuit constructed by the amplifier transistor 115 provided in the pixel circuit 110 and the load transistor 101 provided in the load circuit, and does not necessarily become the same as the electric potential of the GND.

As can be seen from FIG. 13, in the case of DC driving the clip transistor 131, a path on which a current flows from the GND to the CLIPDC is formed. The DC drive therefore has a problem of high power consumption.

<Operation 2>

The following describes the operation when the clip transistor 131 is pulse driven.

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FIG. 14A shows the state of electric potential in each area of the signal processing circuit 130 at the timing "d" in FIG. 12 in the high brightness case.

FIG. 14B shows the state of electric potential in each area of the signal processing circuit 130 at the timing "e" in FIG. 12 in the high brightness case.

Here, FIGS. 14A and 14B each show in its upper half a schematic circuit configuration and in its lower half the state of electric potential in the areas corresponding to the positions in the circuit shown in the upper half.

The following describes the state of electric potential in each area of the signal processing circuit 120 in the high brightness case, with reference to FIGS. 14A and 14B.

(1) At the timing "d" in FIG. 12, as shown in FIG. 14A, the charge of the GND exceeds the barrier potential of the load transistor 101 and is transferred to the first signal output line. Because the sampling transistor 121 is ON and the clip transistor 131 is OFF, the charge sequentially exceeds the barrier potential of each transistor and is transferred to the second signal output line.

Here, the electric potential of the first signal output line is determined by a source follower circuit constructed by the amplifier transistor 115 provided in the pixel circuit 110 and the load transistor 101 provided in the load circuit, and does not necessarily become the same as the electric

potential of the GND.

(2) At the timing "e" in FIG. 12, as shown in FIG. 14B, the charge of the GND exceeds the barrier potential of the load transistor 101 and is transferred to the first signal output line. Because the sampling transistor 121 is OFF and the clip transistor 131 is ON, the charge sequentially exceeds the barrier potential of each transistor at the right side of the sampling transistor 121 and is transferred, but this charge transfer stops when the voltage of each signal line reaches a voltage that is determined by the barrier potential of each transistor. Here, the voltage of the second signal output line can be set by the pulse voltage of the clip transistor 131.

As can be seen from FIGS. 14A and 14B, in the case of pulse driving the clip transistor 131, a path where a current flows from the GND to the CLIPDC is not formed. The pulse drive therefore is advantageous in its smaller power consumption than the DC drive.

<Conclusions>

In the second embodiment described above, the clip transistor 131 is added to the construction of the imaging device relating to the first embodiment. In the second embodiment, therefore, the voltage of the second signal output line can be set so as not to reach a voltage exceeding an

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input dynamic range of an output amplifier of the subsequent stage.

[Third Embodiment]

<Construction>

FIG. 15 shows a schematic circuit configuration of an imaging device relating to a third embodiment of the present invention.

As shown in FIG. 15, the imaging device relating to the third embodiment includes, instead of the pixel circuit 110 and the signal processing circuit 120 in the first embodiment, a pixel circuit 140 and a signal processing circuit 150.

The pixel circuit 140 is characterized by outputting a reset voltage obtained by amplifying a voltage at reset and a read voltage obtained by amplifying a voltage at reading, to the first signal output line. The pixel circuit 140 includes a light-receiving element 141 such as a photodiode that subjects incident light to photoelectric conversion to generate and accumulate charge and outputs the accumulated charge as a voltage signal, a reset transistor 142 that discharges the accumulated charge in the light-receiving element 141 and resets the voltage therein to an initialization voltage (VDD here), an amplifier transistor 143 that outputs a voltage that follows the voltage indicated by the charge accumulated in the light-receiving element 141, and a line

select transistor 144 that outputs an output of the amplifier transistor 143 to the first signal output line upon receipt of a line select signal from the line select encoder 3.

Here, to the pixel circuit 140, a reset pulse (initialization signal: RESET) and a line select pulse (line select signal: LSEL) are supplied at predetermined timings, and to the signal processing circuit 150, a sampling pulse (SP) and a clamp pulse (CP) are supplied at predetermined timings. Transistors corresponding to these control pulses are switched ON and OFF.

The signal processing circuit 150 includes the same components as those of the signal processing circuit 120 in the first embodiment. The signal processing circuit 150 is the same as the signal processing circuit 120 in the first embodiment except that the clamp transistor 124 is connected in series between the second signal output line and a voltage terminal VCL for a clamp in the signal processing circuit 150 whereas the clamp transistor 124 is connected in series between the second signal output line and the reference voltage terminal VDD in the signal processing circuit 120.

Here, it is preferable to set the electric potential of the voltage terminal VCL for a clamp a little higher than the barrier potential $V\phi SKIP$ of the bypass transistor 125, specifically at around $VCL=V\phi SKIP+0.1V$", so that the electric potential of the second signal output line does not exceed

the barrier potential of the bypass transistor 125 when the clamp transistor 124 is switched ON.

Here, the electric potential of the *VCL* may be set by incorporating a depletion-mode transistor as the clamp transistor 124 during the manufacture, or by supplying, with the use of voltage supplying means, a bias voltage constantly or at necessary timings ("c" to "d" in FIG. 16 etc.) to the gate of the clamp transistor 124.

As one example, the bias voltage may be output, in the form of pulses, to the gate of the clamp transistor 124 during when the read voltage is being read from the pixel circuit 140.

FIG. 16 shows the timings of various control pulses supplied in the imaging device relating to the third embodiment.

By supplying the control pulses at the timings shown in FIG. 16, the clamp transistor 124 can be switched ON with the line select transistor 116 being ON, and the second signal output line can be set to the reference voltage with the first signal output line outputting the read voltage ("a" in FIG. 16). Here, when the read voltage is in a predetermined range, an equivalent to a difference between the read voltage and the reference voltage is held by the clamp capacitance 122. After this, the first signal output line outputs the reset voltage ("c" in FIG. 16) with the clamp transistor 124 being

OFF ("b" in FIG. 16). The voltage of the second signal output line changes by an amount equivalent to a difference between the reset voltage and the read voltage ("d" in FIG. 16). The resulting voltage can then be output as brightness information.

5   When the read voltage is not in a predetermined range, the bypass transistor 125 brings the first signal output line and the second signal output line into conduction to bypass the clamp capacitance 122, so that there is no difference between the first signal output line and the second signal

10 output line and no charge is held by the clamp capacitance 122. After this, the voltage of the second signal output line is replaced by the reset voltage. The resulting voltage can be output as brightness information.

Here, the predetermined voltage range may be set by

15 incorporating a depletion-mode transistor as the bypass transistor 125 during the manufacture, or by supplying, with the use of voltage supplying means, a bias voltage constantly or at necessary timings ("c" to "d" in FIG. 16 etc.) to the gate of the bypass transistor 125.

20   As one example, the bias voltage may be output, in the form of pulses, to the gate of the bypass transistor 125 during when the read voltage is being read from the pixel circuit 110.

25 <Operations>

FIGS. 17A to 17D each show the state of electric potential in each area of the pixel circuit 140 at each timing in the normal case.

FIGS. 17A to 17D respectively correspond to the timings "a" to "d" in FIG. 16.

FIG. 18A shows the state of electric potential in each area of the signal processing circuit 150 at the timing "a" in FIG. 16.

FIG. 18B shows the state of electric potential in each area of the signal processing circuit 150 at the timing "b" in FIG. 16.

FIG. 18C shows the state of electric potential in each area of the signal processing circuit 150 at the timing "d" in FIG. 16.

Here, FIGS. 17A to 17D and FIGS. 18A to 18C each show in its upper half a schematic circuit construction and in its lower half the state of electric potential in the areas corresponding to the positions in the circuit shown in the upper half.

The following describes the change of electric potential in each area of the pixel circuit 140 and the change of electric potential in each area of the signal processing circuit 150, with reference to FIGS. 17A to 17D and FIGS. 18A to 18C.

(1) At the timing "a" in FIG. 16, the reset transistor 142 is OFF, and the voltage of the light-receiving element

141 changes due to the charge generated therein as shown in FIG. 17A. Because the line select transistor 144 is ON, the resulting voltage is amplified by the amplifier transistor 143, and the voltage of the first signal output line changes to the read voltage. Also, because the clamp transistor 124 is ON, the voltage of the second signal output line is reset to the *VCL* as shown in FIG. 18A.

Here, the barrier potential *VϕSKIP* of the bypass transistor 125 is assumed to be about 0.7V, the voltage terminal *VCL* for a clamp to be about 0.8V, and the read voltage output to the first signal output line as one example to be about 1.5V.

(2) At the timing "b" in FIG. 16, the clamp transistor 124 is switched from ON to OFF. As shown in FIG. 18B, an equivalent to a difference between the read voltage and the *VCL* is held by the clamp capacitance 122.

Here, as one example, an equivalent to a difference of about 0.7V between the read voltage of about 1.5V and the *VCL* of about 0.8V is held by the clamp capacitance 122.

(3) At the timing "c" in FIG. 16, the reset transistor 142 is switched ON. Therefore, as shown in FIG. 17C, the charge generated in the light-receiving element 141 is transferred to the *VDD* terminal.

(4) At the timing "d" in FIG. 16, the reset transistor 142 is switched from ON to OFF. As shown in FIG. 17D, the

voltage of the light-receiving element 141 is reset to the *VDD*.

Here, the voltage of the light-receiving unit 141 changes to the *VDD*, and the resulting voltage is amplified by the amplifier transistor 115. Therefore, the voltage of the first signal output line changes to the reset voltage. Also, because the equivalent to the difference between the read voltage and the *VCL* is held by the clamp capacitance 122, the voltage of the second signal output line becomes a voltage obtained by subtracting the voltage change of the first signal output line from the *VCL* as shown in FIG. 16C. The resulting voltage is then output as brightness information (assuming the voltage change of the first signal output as *SIG*, the clamp capacitance 122 as *Ccp*, and the sampling capacitance 123 as *Csp*, the voltage of the second signal output line is $VCL+SIG \times Ccp/(Ccp+Csp)$).

Here, assuming as one example the reset voltage *Vreset* output to the first signal output line to be about 2.0V and $Ccp=Csp$, the voltage *Vnrm* of the second signal output line becomes

$$Vnrm=VCL+SIG \times Ccp/(Ccp+Csp)$$
$$=0.8+(2.0-1.5) \times (1/2)=1.05(V)".$$

FIGS. 19A to 19D each show the state of electric potential in each area of the pixel circuit 140 at each timing in the high brightness case.

Here, FIGS. 19A to 19D respectively correspond to the

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timings shown in FIG. 16A to 16D.

FIG. 20A shows the state of electric potential in each area of the signal processing circuit 150 at the timing "a" in FIG. 16 in the high-brightness case.

FIG. 20B shows the state of electric potential in each area of the signal processing circuit 150 at the timing "b" in FIG. 16 in the normal case.

FIG. 20C shows the state of electric potential in each area of the signal processing circuit 150 at the timing "d" in FIG. 16 in the normal case.

Here, FIGS. 19A to 19D and FIGS. 20A to 20C each show in its upper half a schematic circuit construction and in its lower half the state of electric potential in the areas corresponding to the positions in the circuit shown in the upper half.

The following describes the change of electric potential in each area of the pixel circuit 140 and the change of electric potential in each area of the signal processing circuit 150, with reference to FIGS. 19A to 19D and FIGS. 20A to 20C.

(1) At the timing "a" in FIG. 16, the reset transistor 142 is OFF. As shown in FIG. 19A, the voltage of the light-receiving element 141 changes due to the charge generated therein. Because the line select transistor 144 is ON, the resulting voltage is amplified by the amplifier transistor 143, and the voltage of the first signal output

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line changes to the read voltage. Also, because the clamp transistor 124 is ON, the voltage of the second signal output line is reset to the *VCL*.

Here, the barrier potential $V\phi SKIP$ of the bypass transistor 125 is assumed to be about 0.7V, the voltage terminal *VCL* for a clamp to be about 0.8V, and the read voltage output to the first signal output line as one example to be about 0.5V.

(2) At the timing "b" in FIG. 16, the clamp transistor 124 is switched from ON to OFF. Here, in the normal case, an equivalent to a difference between the read voltage and the reference voltage is held by the clamp capacitance 122. In the high brightness case as shown in FIG. 20B, however, the barrier potential of the read transistor exceeds the barrier potential of the bypass transistor 125 and the bypass transistor 125 brings the first signal output line and the second signal output line into conduction to bypass the clamp capacitance 122. Therefore, no charge is held by the clamp capacitance 122.

Here, as one example, a read voltage of about 0.5V exceeds a $V\phi SKIP$ of about 0.7V, and therefore, the voltage of the first signal output line and the voltage of the second signal output line both become about 0.5V. No charge is therefore held by the clamp capacitance 122.

(3) At the timing "c" in FIG. 16, the reset transistor

142 is switched ON.   As shown in FIG. 19C, therefore, the charge generated in the light-receiving element 141 is transferred to the *VDD* terminal.

(4) At the timing "d" in FIG. 16, although the reset transistor 142 is switched from ON to OFF, as shown in FIG. 19D, the light-receiving element 141 outputs a voltage a little lower than the *VDD*, due to the charge generated in the high brightness case.

Here, because no charge is held by the clamp capacitance 122, as shown in FIG. 20C, the voltage of the second signal output line becomes an equivalent to the reset voltage, indicating high brightness.   The resulting voltage is then output as brightness information.

To be more specific, when the voltage of the first signal output line exceeds the barrier potential of the bypass transistor, the voltage of the first signal output line is equal to the voltage of the second signal output line.   When the voltage of the first signal output line is higher than the barrier potential of the bypass transistor, the voltage of the second signal output line changes at a ratio fixed by the sampling capacitance *Csp* and the clamp capacitance *Ccp* with respect to the voltage change of the first signal output line.   The voltage *Vov* of the second signal output line at this time is written as

$$Vov = V\phi SKIP + (Vreset - V\phi SKIP) \times Ccp/(Ccp + Csp).$$

Here, assuming as one example the reset voltage *Vreset* output to the first signal output line to be about 1.9V and *Ccp=Csp*, the voltage *Vov* of the second signal output line becomes

5   *Vov=VϕSKIP+(Vreset−VϕSKIP)xCcp/(Ccp+Csp)*

    =0.7+(1.9−0.7)x(1/2)=1.3(V).

In the above example, the inequality *Vov>Vnrm* is satisfied.

However, when *VCL>>VϕSKIP*, the inequality *VoV>Vnrm* is
10 not satisfied. Therefore, a difference between the *VCL* and the *VϕSKIP* needs to be in such a range that satisfies the inequality *VoV>VϕSKIP* as in the above example. As one example, it is preferable that the *VCL* is about 0.8V and the *VϕSKIP* is about 0.7V with the difference between the *VCL* and the
15 *VϕSKIP* being about 0.1V.

<Conclusions>

The imaging device relating to the third embodiment has the same output voltage characteristics as those of the imaging
20 device relating to the first embodiment. When the read voltage exceeds a predetermined voltage, the output voltage is replaced by a voltage indicating high brightness. Therefore, underexposure or shadow detail loss of an image can be prevented, and the same effects as produced in the first embodiment can
25 be produced in the third embodiment.

[Modification 1]

FIGS. 21A and 21B show the relationship between the barrier potential of the reset transistor and the barrier potential of the bypass transistor.

The following describes the relationship between the barrier potential $V\phi R$ of the reset transistor and the barrier potential $V\phi SKIP$ of the bypass transistor.

Here, an amplification factor of the amplifier transistor is assumed to be α and a threshold voltage is assumed to be Vt.

As shown in FIG. 21A, when the $V\phi SKIP$ is set equal to or smaller than the minimum potential $Vmin=(V\phi R-Vt)\times\alpha$ of the first signal output line determined by the $V\phi R$ ($V\phi SKIP/\alpha+Vt\leqq V\phi R$), the saturation signal $Vsat$ becomes $Vsat=VDD-V\phi R$, so that the maximum virtual electric potential of the saturation signal output can be secured. However, the bypass transistor is not switched ON in the high brightness case, and therefore the bypass transistor does not work.

As shown in FIG. 21B, when the $V\phi SKIP$ is set larger than the minimum potential $Vmin=(V\phi R-Vt)\times\alpha$ of the first signal output line determined by the $V\phi R$ ($V\phi SKIP/\alpha+Vt>V\phi R$), the saturation signal $Vsta$ becomes $Vsta=VDD-(V\phi SKIP/\alpha+Vt)$. When a difference between the $V\phi SKIP$ and the $Vmin$ is larger than a predetermined value, the bypass transistor

works. However, the virtual electric potential of the saturation signal output decreases as this difference increases.

Here, it is preferable that the difference between the $V\phi SKIP$ and the $Vmin$ is about 0.1V.

It should be noted here that the bypass transistor and the reset transistor may be manufactured in one process, and the bias voltage may be supplied to the gate of the bypass transistor. Here, the difference between the barrier potential of the bypass transistor and the electric potential of the saturation signal output may be set using the bias voltage.

Also, the reset transistor may be manufactured by a predetermined process of burying it through injection, and the bypass transistor may be manufactured by the predetermined process of burying it through injection and an additional injection process. Here, the difference between the barrier potential of the bypass transistor and the electric potential of the saturation signal output may be set using the bias voltage.

<Conclusions>

According to the modification 1 as described above, a sufficient level of the virtual electric potential of the saturation signal output can be secured, and also, the bypass

transistor can work, thereby producing an expected effect.

[Modification 2]

For the imaging device, a vertical blanking period,
during which brightness information of a predetermined number
of pixels is not output from the imaging unit, is provided
for each frame.

If the imaging device is driven during the vertical
blanking period in the same manner as in normal periods, the
electric potential of the first signal output line becomes
0V due to the load circuit, and a saturation signal is
excessively output during the vertical blanking period. The
problem here is that an input dynamic range of an output
amplifier of the subsequent stage is restricted, and a small
signal cannot be sufficiently amplified.

To solve this problem, the modification 2 of the present
invention provides an imaging device that does not output
a saturation signal during the vertical blanking period, an
imaging method, and the like.

FIG. 22 shows the timings of a sampling pulse in the
modification 2.

The sampling pulse shown in FIG. 22 is an output example
in an imaging device that has the same construction as the
imaging device relating to the first embodiment. The sampling
pulse is assumed to be output from the sampling transistor

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control unit included in the column select encoder 4.

As shown in FIG. 22, the sampling transistor control unit does not output a sampling pulse during the vertical blanking period. Therefore, the sampling transistor 121 is brought out of conduction, and no charge is held by the clamp capacitance 122. As a result, brightness information indicating low brightness is output.

<Conclusions>

According to the modification 2 as described above, a saturation signal is not output during the vertical blanking period, and therefore an input dynamic range of an output amplifier of the subsequent stage is not restricted.

[Modification 3]

To solve the same problem as dealt with by the modification 2, the modification 3 of the present invention provides an imaging device that does not output a saturation signal during the vertical blanking period, an imaging method, and the like.

FIG. 23 shows the timings of a sampling pulse in the modification 3.

The control over the gate voltage of the load transistor shown in FIG. 23 is a control example in an imaging device that has the same construction as the imaging device relating

to the first embodiment. The control is assumed to be performed by the load transistor control unit included in the column select encoder 4.

As shown in FIG. 23, the load transistor control unit does not apply a bias voltage to the load transistor during the vertical blanking period. Therefore, the load transistor 101 is brought out of conduction, and no charge is held by the clamp capacitance 122. As a result, brightness information indicating low brightness is output.

<Conclusions>

According to the modification 3 as described above, a saturation signal is not output during the vertical blanking period, and therefore an input dynamic range of an output amplifier of the subsequent stage is not restricted.

It should be noted here that each circuit used to describe the present invention is a mere example, and other circuits and the like having the same functions as the above-described circuits may instead be used.

Also, instead of each signal processing circuit, a general-purpose processor may be used to separately measure the reset voltage and the read voltage, and realize the processing performed by each signal processing circuit based on the measurement results. Alternatively, the imaging device may be operated using a conventional signal processing

circuit in the normal case, and may be operated using a general-purpose processor in the case judged as the high brightness case when the read voltage is not in a predetermined range and may replace the output signal by a voltage indicating high brightness in the high brightness case.

Also, to set the bias voltages supplied by the voltage supplying means to the gates of the clamp transistor, the bypass transistor, etc., at appropriate values for an individual imaging device, the voltage supplying means may include a bias voltage setting circuit that enables each bias voltage to be set from outside and that can store the set value of each bias voltage.

This bias voltage setting circuit includes, for each transistor to which the bias voltage is to be supplied, a plurality of parallel-connected wires made of polysilicon or the like that can be disconnected by for example applying a predetermined voltage to their specific terminals from outside, and includes elements that are connected to the wires and that can change a voltage of the same or different resistance or the like. In the final stage of the manufacturing, appropriate ones of the wires are disconnected in such a manner that the electric potential of the connected transistor is set at an optimum value by monitoring the output data. As one example, to set a difference between the barrier potential of the bypass transistor and the electric potential of the

saturation signal output at an optimum value, appropriate
ones of the wires may be disconnected in such a manner that
the bias voltage of the bypass transistor is set at an optimum
value by monitoring the voltage of the second signal output
line.

Also, although the above embodiments and modifications
of the present invention describe the case where the signal
charge is realized by an electron, the signal charge may be
realized by an electron hole. When the signal charge is
realized by an electron hole, the signal polarity is inverse
and the magnitude relation of the electric potential is the
opposite, compared with when the signal charge is realized
by an electron.

Although the above embodiments and modifications of the
present invention describe the case where a MOS amplifier
transistor is used, the present invention can be realized
by using an imaging device that requires a circuit for removing
FPN (fixed pattern noise) such as CMD, BASIS, and SIT.

[Industrial Application]

The present invention is applicable to imaging devices
such as home video cameras and digital still cameras. The
present invention provides a solid-state imaging device that
can effectively solve the problem of shadow detail loss of
an image underexposed due to incident strong light compared

with conventional devices, and that can ensure elimination of an adverse effect by a change in a voltage at reset, and thereby contributing to improvement in image quality of imaging devices.

5   The present invention is applicable not only to home imaging devices but also to any other types of imaging devices.

Although the present invention has been fully described by way of examples with reference to the accompanying drawings, 10   it is to be noted that various changes and modifications will be apparent to those skilled in the art. Therefore, unless such changes and modifications depart from the scope of the present invention, they should be construed as being included therein.